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ABSTRACT OF THE DISCLOSURE

L-shaped spacers for use adjacent to the vertical sidewalls of gate electrodes in the manufacture of MOS integrated circuits are described along with methods of fabricating such structures that do not require any additional cost compared to conventional manufacturing processes. A spacer is formed as a tri-layer of silicon oxide/silicon nitride/silicon oxide deposited in-situ at low temperature using a conventional furnace and a bis(tertiarybutylamino) silane chemistry deposition. The spacer has the same performance as a conventional spacer during deep source/drain (S/D) implants. Prior to a cleaning operation which precedes silicidation, the top oxide layer is removed leading to improved gap-fill characteristics. The upper oxide may be removed before deep S/D implantation to further achieve reduction of series resistance.